REMARKS

Claims 1-22 are pending in the application.

Claims 1, 10, 14, 21 and 22 were amended herein.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claim 22 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. Specifically, the Office Action states that "the hash function" lacks antecedent basis. In response, the Applicants have amended claim 22 to correct this error.

Therefore, the rejection of claim 22 under 35 U.S.C. § 112, second paragraph has been overcome.

35 U.S.C. § 103 (Obviousness)

Claims 1-3, 5-16 and 18-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,665,297 to *Hariguchi, et al* in view of U.S. Patent Publication No. 2001/0027479 to *Delaney et al.* Claims 4 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hariguchi* in view of *Delaney* and further in view of U.S. Patent No. 6,625,612 to *Tal et al.* These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-127 (8th ed. rev. 7 July 2008). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a prima facie case of obviousness, three basic criteria must be met: First, there must be some reason – such as a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art – to modify the reference or to combine reference teachings. MPEP § 2142, pp. 2100-127 to 2100-128 (8th ed. rev. 7 July 2008); MPEP § 2143, pp. 2100-128 to 2100-139; MPEP § 2143.01, pp. 2100-139 to 2100-141. Second, there must be a reasonable expectation of success. MPEP § 2143.02, pp. 2100-141 to 2100-142 (8th ed. rev. 7 July 2008). Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. MPEP § 2143.02, pp. 2100-141 to 2100-142 (8th ed. rev. 7 July 2008).

Independent claims 1 and 10 each recite "a configuration register associated with each memory block, each configuration register identifying a prefix length to which the respective memory block is allocated." Similarly, independent claim 14 recites that "each memory block is associated with a configuration register that identifies a prefix length to which the memory block is allocated." These features -- adapted from claim 21, previously indicated (page 9 of the Office Action dated June 26, 2008) to be allowable if rewritten in independent form and to overcome the § 112 rejection -- are not found in the cited references.

. This Office Action asserts that the mask circuit 154 in *Hariguchi* teaches this feature. However, the portion of *Hariguchi* cited in the Office Action actually reads:

> Each mask circuit 154 outputs the high order bits of the network portion of the destination address that correspond to the prefix length for that hash circuit 82. For example, the mask circuit for hash circuit 82-8 (FIG. 2) will output the leading eight bits of the network portion of the destination address, while the mask circuit for hash circuit 82-32 (FIG. 2) will output all thirty-two bits of the network portion of the destination address. (Hariguchi, col. 6, lns. 54-61).

According to this passage, the mask circuit 154 is used to strip off lower order bits from the network

portion of a destination address, and then output only the high order bits in the hash circuit 82. From this passage, it is clear that a mask circuit is not equivalent to a configuration register. Furthermore, nothing in this passage teaches or suggests that a mask circuit is associated with each memory block. Nor does the passage teach that each mask circuit identifies the prefix length or hash function to which a memory block is allocated. In fact, the passage doesn't say anything at all about memory blocks. No other part of *Hariguchi* teaches or suggests a configuration register associated with each memory block, each configuration register identifying a prefix length to which the respective memory block is allocated. *Delaney* and *Tal* fail to cure the deficiencies of *Hariguchi*.

Therefore, the rejection of claims 1-22 under 35 U.S.C. § 103 has been overcome.

If any issues arise or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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